An introduction to POWER8 processor
Technology Rises: key external factor for CEOs
Three most important “external” forces over the next 3 years
For the first time, CEOs identify technology as the most important external force impacting their organizations

Source: Q1 IBM CEO study 2012 “What are the most important external forces that will impact your organization over the next 3 to 5 years?”
Outperforming organizations focused on combining technology with the business to drive innovation and growth.

Integrating business and technology for innovation

“The biggest risk we face is technological. If we fail to anticipate a huge technology step, we might go out of business.”

Industrial Products CEO, France

“How do you unleash the innovative power of the people who deal with your customers every day?”

Insurance CEO, United Kingdom

Source: QE “To what extent has your organization integrated business and technology to innovate?”
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Business needs are Transforming ➔ Driving infrastructure Transformation

69% of IT cost is server management & administration (est $247B)

8 zettabytes digital content by 2015 (90% unstructured)

Databases

Applications

Instrumented Devices & Sensors

Mobile

Social

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80% of new applications will be developed with cloud characteristics

1 Trillion Connected devices by 2015

25+ average # of mobility applications to be deployed by CIOs in next 2 years

Client Business needs have evolved

- Data-driven insights
- Flexible, responsive IT environment
- Secure from external and internal threats
- Simplified end user experience
- Compelling ROI

1 ZB = 1000000000000000000000000 bytes
= 1000^7 bytes = 10^21 bytes = 1000 exabytes = 1 billion terabytes
The rise of new workloads
POWER8 designed for the next generation of demanding workloads

- Systems of Engagement
  - Social networking
  - Collaborative

- Systems of Record
  - Database
  - ERP
  - OLTP

- Cognitive Systems
  - Dynamic learning
  - Watson 2.0

- Static Data
  - Analytics
  - Modelling

- Data in Motion
  - Real-time analytics
  - Instrumentation
POWER8 Processor
POWER8 Vision

**Leadership Performance**
- Increase core throughput at single thread, SMT2, SMT4, and SMT8 level
- Large step in per socket performance
- Enable more robust multi-socket scaling

**System Innovation**
- Higher capacity cache hierarchy and highly threaded processor
- Enhanced memory bandwidth, capacity, and expansion
- Dynamic code optimization
- Hardware-accelerated virtual memory management

**Open System Innovation**
- Coherent Accelerator Processor Interface (CAPI)
- Agnostic Memory interface
- Open system software

Optimize Analytics & Big Data
Enhance Cloud Efficiency
Enable Open Innovation on POWER
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POWER8 Processor

Technology
- 22nm SOI, eDRAM, 15 ML 650mm2

Caches
- 512 KB SRAM L2 / core
- 96 MB eDRAM shared L3
- Up to 128 MB eDRAM L4 (off-chip)

Memory
- Up to 230 GB/s sustained bandwidth

Bus Interfaces
- Durable open memory attach interface
- Integrated PCIe Gen3
- SMP Interconnect
- CAPI (Coherent Accelerator Processor Interface)

Cores
- 12 cores (SMT8)
- 8 dispatch, 10 issue, 16 exec pipe
- 2X internal data flows/queues
- Enhanced prefetching
- 64K data cache, 32K instruction cache

Accelerators
- Crypto & memory expansion
- Transactional Memory
- VMM assist
- Data Move / VM Mobility

Energy Management
- On-chip Power Management Micro-controller
- Integrated Per-core VRM
- Critical Path Monitors
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POWER8 Core
An introduction to POWER8 processor

POWER8 Core

Execution Improvement vs. POWER7
- SMT4 → SMT8
- 8 dispatch
- 10 issue
- 16 execution pipes:
  - 2 FXU, 2 LSU, 2 LU, 4 FPU,
    2 VMX, 1 Crypto, 1 DFU,
    1 CR, 1 BR
- Larger Issue queues (4 x 16-entry)
- Larger global completion, Load/Store reorder
- Improved branch prediction
- Improved unaligned storage access

Larger Caching Structures vs. POWER7
- 2x L1 data cache (64 KB)
- 2x outstanding data cache misses
- 4x translation Cache

Wider Load/Store
- 32B → 64B L2 to L1 data bus
- 2x data cache to execution dataflow

Enhanced Prefetch
- Instruction speculation awareness
- Data prefetch depth awareness
- Adaptive bandwidth awareness
- Topology awareness

Core Performance vs. POWER7
- ~1.6x Thread
- ~2x Max SMT
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POWER8 Core

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POWER8 On-chip Caches

- **L2**: 512 KB 8 way per core
- **L3**: 96 MB (12 x 8 MB 8 way Bank)
- **“NUCA” Cache policy** (Non-Uniform Cache Architecture)
  - Scalable bandwidth and latency
  - Migrate “hot” lines to local L2, then local L3 (replicate L2 contained footprint)
- **Chip Interconnect**: 150 GB/sec x 12 segments per direction = 3.6 TB/sec
Cache Bandwidth

- GB/sec shown assuming 4 GHz
  Product frequency will vary based on model type

- Across 12 core chip
  4 TB/sec L2 BW
  3 TB/sec L3 BW
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Memory Organization

- Up to 8 high speed channels, each running up to 9.6 Gb/s for up to 230 GB/s sustained
- Up to 32 total DDR ports yielding 410 GB/s peak at the DRAM
- Up to 1 TB memory capacity per fully configured processor socket
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**Memory Buffer Chip** …with 16MB of Cache…

**Intelligence Moved into Memory**
- Scheduling logic, caching structures
- Energy Mgmt, RAS decision point
  - Formerly on Processor
  - Moved to Memory Buffer

**Processor Interface**
- 9.6 GB/s high speed interface
- More robust RAS
- “On-the-fly” lane isolation/repair
- Extensible for innovation build-out

**Performance Value**
- End-to-end fastpath and data retry (latency)
- Cache → latency/bandwidth, partial updates
- Cache → write scheduling, prefetch, energy
- 22nm SOI for optimal performance / energy
- 15 metal levels (latency, bandwidth)
Centaur Memory DIMM
2-hop Interconnect

48-way Drawer

38.4 GB/s

12.8 GB/s
P7 Routing

P7 node to node peak is 20 GB/sec
Source $\to$ Target Bandwidth = 12.8 GB/sec

P7 node to node peak is 20 GB/sec
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+Secondary Route

Source

Target

Source → Target Bandwidth = 25.6 GB/sec  P7 node to node peak is 20 GB/sec
Source $\rightarrow$ Target Bandwidth = 51.2 GB/sec  
P7 node to node peak is 20 GB/sec
Source → Target Bandwidth = 153.6 GB/sec  P7 node to node peak is 20 GB/sec
Socket Performance

- POWER7+ baseline
- Memory Bandwidth
- Commercial
- Java
- Integer
- Floating Point
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Integrated PCIe Gen3

Native PCIe Gen 3 Support
- Direct processor integration
- Replaces proprietary GX/Bridge
- Low latency
- Gen3 x16 bandwidth (16 Gb/s)

Transport Layer for CAPI Protocol
- Coherently Attach Devices connect to processor via PCIe
- Protocol encapsulated in PCIe
CAPI Coherent Accelerator Processor Interface

Virtual Addressing
- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead

Hardware Managed Cache Coherence
- Enables the accelerator to participate in “Locks” as a normal thread
- Lowers Latency over IO communication model

Customizable Hardware Application Accelerator
- Specific system SW, middleware, or user application
- Written to durable interface provided by PSL

Processor Service Layer (PSL)
- Present robust, durable interfaces to applications
- Offload complexity / content from CAPP

Custom Hardware Application
- FPGA or ASIC

POWER8 Coherence Bus

PCIe Gen 3
Transport for encapsulated messages
## Technology

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<td>1.9MB 36MB</td>
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<td>2 + 32MB None</td>
<td>2 + 80MB None</td>
<td>6 + 96MB 128MB</td>
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<td>30GB/s 20GB/s</td>
<td>100GB/s 40GB/s</td>
<td>100GB/s 40GB/s</td>
<td>230GB/s 96GB/s</td>
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## Compute
- Cores
- Threads

## Caching
- On-chip
- Off-chip

## Bandwidth
- Sust. Mem.
- Peak I/O

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POWER8 Enabling: …Big Data, Analytics, Cognitive Computing…

POWER8 Differentiation for Analytics

- Massive capacity and bandwidth to memory and IO
- Large caches with massive bandwidth
- Strong Single thread
- SMT8, Many threads to hide memory latency
  - Graph traversals
  - Transactional memory enables efficient thread scaling

CAPI Accelerators

- Enables heterogeneous compute (GPU, FPGA, etc.)

Synergy with IBM Software, Driving Optimization Across the Stack
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**POWER8 Highlights**

**PERFORMANCE**

- The Register: “it most certainly does belong in a **badass** server, and Power8 is by far one of the most elegant chips that Big Blue has ever created”
- Huge performance improvement:
  - 1.5X to 1.7X thread-level improvement*
  - 2X core improvement*
  - 3X socket improvement*
- Compared with POWER7+
  - Commercial 2.5X* and Java 2.6X*
  - Integer 2.2X* and Floating Point 2.3X*
- Coherent Accelerators (CAPI) – memory-space addressable
- SMP scaling
  - 16 sockets, 192 cores
  - Lower latency, high speed
POWER8 Highlights
MEMORY and BANDWIDTH

- Linley Group microprocessor report: “The Power8 specs are mind boggling. . .IBM’s newest server processor will smash existing performance records, particularly for memory-intensive applications”

- Caching Structure
  - L1 to L4 cache with Non-Uniform Cache Architecture
  - 4 TB/s L2 bandwidth* per chip (4GHz 12core)
  - 3 TB/s L3 bandwidth* per chip (4GHz 12core)

- Memory Subsystem
  - 230 GB/s sustained* bandwidth per chip
  - 410 GB/s bandwidth* at DRAM level per chip
  - 1 TB memory per socket (e.g. 4sockets = 4 TB)
  - Transactional Memory
POWER8 Highlights
I/O, BANDWIDTH, VALUE

- TechInvestor/VentureBeat: “IBM preps its massive 12-headed Power 8 chip”
- Balance I/O capability
  - PCIe Gen3 on-chip I/O connectivity and protocol (Low latency)
  - I/O bandwidth 96 GB/s per socket
  - Flexible chip interface
- Energy 3X capacity per watt improvement*
- Improved RAS
- P6/P7/P8 modes and Live Partition Mobility
- Workload density / LPAR density

* approximate
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- Significant Performance at Thread, Core, and System
- Optimization for VM Density & Efficiency
- Strong Enablement of Autonomic System Optimization
- Excellent Big Data Analytics Capability

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POWER8 Microprocessor

“certainly does belong in a badass server”

QUESTIONS
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